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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,200	12/30/2003	Swaminathan Sivakumar	42P17540	9156

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EXAMINER	
CHEN, ERIC BRICE	
ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,200	SIVAKUMAR ET AL.	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *16-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-21* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-15, drawn to method, classified in class 438, subclass 689.

II. Claims 16-21, drawn to a silicon substrate, classified in class 428, subclass E21.579.

2. The inventions are distinct, each from the other because of the following reasons: Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the sloped sidewall of the silicon substrate can be formed by methods other than heating, such as uneven light exposure.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper. Furthermore, because these inventions are distinct for the reasons given above and the search required for Invention I is not required for Invention II, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Michael A. Bernadicou on Aug. 12, 2005, a provisional election was made with traverse to prosecute the Invention I, claims 1-15.

Affirmation of this election must be made by applicant in replying to this Office action. Claims 16-21 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Priority

6. Applicant is advised of possible benefits under 35 U.S.C. 119(a)-(d), wherein an application for patent filed in the United States may be entitled to the benefit of the filing date of a prior application filed in a foreign country.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takagi et al. (U.S. Patent No. 6,174,796), in view of Yu et al. (U.S. Patent No. 6,025,259), in further view of Choi (U.S. Patent No. 6,780,571).

10. As to claim 1, Takagi discloses a method of exposing a bond pad comprising: forming the bond pad (5) over a silicon substrate (1) (column 4, lines 11-15; Figure 3A); forming a dielectric layer (7) over the bond pad (4) and silicon substrate (1) (column 4, lines 19-23; Figure 3A); and forming a resist mask (8) with at least one opening (8a) to expose the dielectric layer over the bond pad (column 4, lines 32-35; Figure 3B).

11. Takagi does not expressly disclose heating the resist mask with the at least one opening to form a sloped sidewall profile in the at least one opening; and etching the resist mask and exposed dielectric layer to form at least one opening in the dielectric layer, having a sloped sidewall profile and exposing the bond pad. However, Takagi teaches forming at least one opening in the dielectric layer, having a sloped sidewall profile (column 2, lines 45-50) in order to avoid the generation of voids in the metal when the opening is filled, thus minimizing resistance (column 3, lines 5-10; Figure 1D). Yu teaches that a sloped sidewall (205) in the resist mask (202) produces a sloped sidewall profile in the underlying dielectric (114), and includes the step of etching the

resist mask (202) and exposed dielectric layer (114) to form at least one opening in the dielectric layer, having a sloped sidewall profile and exposing the bond pad (108) (column 8, lines 20-40; Figures 2G-2H). Furthermore, Choi teaches heating the resist mask (14) with the at least one opening (16) to form a sloped sidewall profile in the at least one opening (16) (column 4, lines 25-39; Figure 1B). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to heat the resist mask with the at least one opening to form a sloped sidewall profile in the at least one opening; and etch the resist mask and exposed dielectric layer to form at least one opening in the dielectric layer, having a sloped sidewall profile and exposing the bond pad. One who is skilled in the art would be motivated to minimize the generation of voids in the metal when the opening is filled, by forming a sloped sidewall and to use a simple method, such as heating the resist and etching, to achieve the sloped profile.

12. As to claim 2, Takagi does not expressly disclose that the heating of the resist mask with the at least one opening persists for a time period ranging from approximately 15 seconds to approximately 90 seconds. However, Choi discloses that the profile of the resist layer can be controlled by varying temperature and time of exposure (column 5, lines 62-67; Figure 2C). Moreover, Choi teaches, by disclosing that the time of exposure may be varied, that changing the time appears to reflect a result-effective variable which can be optimized. *See* MPEP § 2144.05 II. Time of exposure can be varied according, depending on the desired outcome of the sidewall resist mask profile. Therefore, it would have been obvious to one of ordinary skill in the

art at the time the invention was made to heat the resist mask with the at least one opening persists for a time period ranging from approximately 15 seconds to approximately 90 seconds. One who is skilled in the art would be motivated to optimize through routine experimentation of exposure times. *See* MPEP § 2144.05 II.

13. As to claim 3, Takagi does not expressly disclose that the heating of the resist mask with the at least one opening is performed at a temperature ranging from approximately 160 degrees Centigrade to approximately 190 degrees Centigrade. However, Choi discloses that the profile of the resist layer can be controlled by varying temperature and time of exposure (column 5, lines 62-67; Figure 2C). Moreover, Choi teaches, by disclosing that temperature may be varied (Figure 2C), that changing the temperature appears to reflect a result-effective variable which can be optimized. *See* MPEP § 2144.05 II. Temperature can be varied according, depending on the desired outcome of the sidewall resist mask profile. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to heat the resist mask with the at least one opening at a temperature ranging from approximately 160 degrees Centigrade to approximately 190 degrees Centigrade. One who is skilled in the art would be motivated to optimize through routine experimentation of exposure temperature. *See* MPEP § 2144.05 II.

14. As to claim 4, Choi discloses that the sloped sidewall profile of the at least one opening of the resist mask (14) is wider at its upper end relative to its lower end (Figure 1B).

15. As to claim 5, Yu discloses that the sloped sidewall profile of the opening in the dielectric layer (114) is wider at its upper end relative to its lower end (Figures 2G-2I).

16. As to claim 6, Takagi discloses a method of exposing a bond pad comprising: forming the bond pad (5) over a silicon substrate (1) (column 4, lines 11-15; Figure 3A); forming a dielectric layer (7) over the bond pad (4) and silicon substrate (1) (column 4, lines 19-23; Figure 3A); and forming a resist mask (8) with at least one opening (8a) to expose the dielectric layer over the bond pad (column 4, lines 32-35; Figure 3B).

17. Takagi does not expressly disclose heating the resist mask with the at least one opening to form a first sloped sidewall profile of the at least one opening; and etching the resist mask and exposed dielectric layer to form at least one opening in the dielectric layer that exposes the bond pad, the at least one opening in the dielectric layer further comprising a second sloped sidewall profile similar to the first sloped sidewall profile of the at least one opening of the resist mask. However, Takagi teaches forming at least one opening in the dielectric layer, having a sloped sidewall profile (column 2, lines 45-50) in order to avoid the generation of voids in the metal when the opening is filled, thus minimizing resistance (column 3, lines 5-10; Figure 1D). Yu teaches that a sloped sidewall (205) in the resist mask (202) produces a sloped sidewall profile in the underlying dielectric (114), and includes the step of etching the resist mask (202) and exposed dielectric layer (114) to form at least one opening in the dielectric layer, having a sloped sidewall profile and exposing the bond pad (108), the at least one opening in the dielectric layer further comprising a second sloped sidewall profile similar to the first sloped sidewall profile of the at least one opening of the resist mask (column

8, lines 20-40; Figures 2G-2H). Furthermore, Choi teaches heating the resist mask (14) with the at least one opening (16) to form a sloped sidewall profile in the at least one opening (16) (column 4, lines 25-39; Figure 1B). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to heat the resist mask with the at least one opening to form a first sloped sidewall profile of the at least one opening; and etch the resist mask and exposed dielectric layer to form at least one opening in the dielectric layer that exposes the bond pad, the at least one opening in the dielectric layer further comprising a second sloped sidewall profile similar to the first sloped sidewall profile of the at least one opening of the resist mask. One who is skilled in the art would be motivated to minimize the generation of voids in the metal when the opening is filled, by forming a sloped sidewall and to use a simple method, such as heating the resist and etching, to achieve the sloped profile.

18. As to claim 7, Takagi does not expressly disclose that the heating of the resist mask with the at least one opening persists for a time period ranging from approximately 15 seconds to approximately 90 seconds. However, Choi discloses that the profile of the resist layer can be controlled by varying temperature and time of exposure (column 5, lines 62-67; Figure 2C). Moreover, Choi teaches, by disclosing that the time of exposure may be varied, that changing the time appears to reflect a result-effective variable which can be optimized. *See* MPEP § 2144.05 II. Time of exposure can be varied according, depending on the desired outcome of the sidewall resist mask profile. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to heat the resist mask with the at least one

opening persists for a time period ranging from approximately 15 seconds to approximately 90 seconds. One who is skilled in the art would be motivated to optimize through routine experimentation of exposure times. *See* MPEP § 2144.05 II.

19. As to claim 8, Takagi does not expressly disclose that the heating of the resist mask with the at least one opening is performed at a temperature ranging from approximately 160 degrees Centigrade to approximately 190 degrees Centigrade. However, Choi discloses that the profile of the resist layer can be controlled by varying temperature and time of exposure (column 5, lines 62-67; Figure 2C). Moreover, Choi teaches, by disclosing that temperature may be varied (Figure 2C), that changing the temperature appears to reflect a result-effective variable which can be optimized. *See* MPEP § 2144.05 II. Temperature can be varied according, depending on the desired outcome of the sidewall resist mask profile. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to heat the resist mask with the at least one opening at a temperature ranging from approximately 160 degrees Centigrade to approximately 190 degrees Centigrade. One who is skilled in the art would be motivated to optimize through routine experimentation of exposure temperature. *See* MPEP § 2144.05 II.

20. As to claim 9, Choi discloses that the sloped sidewall profile of the at least one opening of the resist mask (14) is wider at its upper end relative to its lower end (Figure 1B).

21. As to claim 10, Takagi discloses that the first sloped sidewall profile of the at least one opening of the resist mask relative to the surface of the silicon substrate

slopes at an angle of approximately 30 degrees to an angle of approximately 60 degrees (column 4, lines 49-56; Figure 3C).

22. As to claim 11, Yu discloses that the forming of a resist mask with at least one opening to expose the dielectric layer over the bond pad exposes only a portion of the bond pad (108) surface (Figure 2I).

23. As to claim 12, Yu does not expressly disclose the forming of a resist mask with at least one opening to expose the dielectric layer over the bond pad exposes the entirety of the bond pad surface. However, Yu teaches that the opening is filled with a conductive material (column 8, lines 37-40; Figure 2J). Thus, exposing the entirely of the bond pad surface increases the surface area, which inherently increases the electrical conductivity of the damascene structure. *See* Callister, *Materials Science and Engineering*, 4th ed., John Wiley & Sons (1997), pages 592-93. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a resist mask with at least one opening to expose the dielectric layer over the bond pad exposes the entirety of the bond pad surface. One who is skilled in the art would be motivated to lower the overall resistance of the device.

24. As to claim 13, Yu discloses that the second sloped sidewall profile of the opening in the dielectric layer (114) is wider at its upper end relative to its lower end (Figures 2G-2I).

25. As to claim 14, Takagi discloses that the second sloped sidewall profile of the opening in the dielectric layer relative to the surface of the silicon substrate slopes at an

angle of approximately 40 degrees to an angle of approximately 50 degrees (column 4, lines 49-56; Figure 3C).

26. As to claim 15, Takagi discloses that the second sloped sidewall profile of the opening in the dielectric layer has a slope sufficient (column 4, lines 49-56; Figure 3C) to facilitate step coverage of a subsequent metallization (column 3, lines 5-10).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC

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Aug. 17, 2005

SUPERVISORY PATENT EXAMINER